WE CLAIM:

1. A semiconductor integrated circuit device on a semiconductor substrate, comprising:

electrically erasable and programmable non-volatile memory elements which store adjustment information;

a memory circuit coupled to receive the adjustment information and to store the adjustment information therein; and

a peripheral circuit coupled to the memory circuit,

wherein the adjustment information is transferred from the electrically erasable and programmable non-volatile memory elements to the memory circuit in response to an initialization operation of the semiconductor integrated circuit device, and then operation of the peripheral circuit is controlled by the adjustment information stored in the memory circuit.

2. A semiconductor integrated circuit device according to claim 1, wherein the memory circuit is a register.

3. A semiconductor integrated circuit device according to claim 1, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit device.

4. A semiconductor integrated circuit device on a semiconductor substrate, comprising:

a memory array including:

first electrically erasable and programmable memory cells, and

second electrically erasable and programmable memory cells which store adjustment information;

a memory circuit which is coupled to receive the adjustment information and which stores the adjustment information therein; and

a peripheral circuit which is coupled to the memory array and which controls a read operation, an erase operation and a programming operation for the memory array, wherein the peripheral circuit is further coupled to the memory circuit,

wherein the adjustment information stored in the second electrically erasable and programmable non-volatile memory cells is read out to the memory circuit in response to an initialization operation of the semiconductor integrated circuit device, and then operation of the peripheral circuit is controlled based upon the adjustment information stored in the memory circuit.

5. A semiconductor integrated circuit device according to claim 4,

wherein the peripheral circuit includes an internal voltage generator which provides internal voltages including an erase voltage and a programming voltage, and

wherein voltage levels of the internal voltage provided from the internal voltage generator are controlled by the adjustment information.

6. A semiconductor integrated circuit device according to claim 4, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit device.

7. A semiconductor integrated circuit device according to claim 4,

wherein the memory circuit is a register.

8. A semiconductor integrated circuit device on a semiconductor substrate, comprising:

first memory cells;

second memory cells which are electrically erasable and programmable non-volatile memory cells and which store adjustment information therein;

a memory circuit coupled to receive the adjustment information and storing the adjustment information therein; and

a peripheral circuit which is coupled to the first memory cells and which controls a read operation and a write operation for the first memory cells, wherein the peripheral circuit is further coupled to the memory circuit,

wherein the adjustment information stored in the second memory cells is read out to the memory circuit in response to an initialization operation of the semiconductor integrated circuit device, and then operation of the peripheral circuit is controlled based upon the adjustment information stored in the memory circuit.

9. A semiconductor integrated circuit device according to claim 8,

wherein the memory circuit is a register.

10. A semiconductor integrated circuit device according to claim 8, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit device.

11. A microprocessor on a semiconductor substrate, comprising:

a bus;

a central processing unit coupled to the bus;

a non-volatile memory which is coupled to the bus and which includes:

a memory array including:

first electrically erasable and programmable memory cells, and

second electrically erasable and programmable memory cells which store adjustment information; and

a peripheral circuit which is coupled to the memory array and which controls a read operation, an erase operation and a programming operation for the memory array; and

a register coupled to receive the adjustment information and to store the adjustment information therein,

wherein the peripheral circuit is further coupled to the memory circuit, and the adjustment information stored in

the second electrically erasable and programmable memory cells is read out to the register in response to an initialization operation of the semiconductor integrated circuit device, and then operation of the peripheral circuit is controlled based upon the adjustment information stored in the register.

12. A microprocessor according to claim 11,

wherein the peripheral circuit includes an internal voltage generator which provides internal voltages including an erase voltage and a programming voltage, and

wherein voltage levels of the internal voltages provided from the internal voltage generator are controlled by the adjustment information.

13. A semiconductor integrated circuit device according to claim 11, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit device.

14. A microprocessor according to claim 11,

wherein the register is coupled to the bus and is accessible from the central processing unit.

15. A microprocessor according to claim 14, wherein the microprocessor has a test mode, and wherein the central processing unit accesses the register to store predetermined data for testing into the register and then the central processing unit programs into the second electrically erasable

and programmable memory cells desired data as the adjustment information.

16. A semiconductor integrated circuit device on a semiconductor substrate, comprising:

electrically erasable and programmable non-volatile memory elements for storing adjustment information;

memory means coupled for receiving the adjustment information and storing the adjustment information therein; and

a peripheral circuit coupled to the memory means,

wherein the adjustment information is transferred from the electrically erasable and programmable non-volatile memory elements to the memory means in response to an initialization operation of the semiconductor integrated circuit device, and then operation of the peripheral circuit is controlled by the adjustment information stored in the memory circuit.

17. A semiconductor integrated circuit device according to claim 16, wherein the memory means is a register.

18. A semiconductor integrated circuit device according to claim 1, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit device.

19. A semiconductor integrated circuit device on a semiconductor substrate, comprising:

a memory array including:

first electrically erasable and programmable memory cells, and

second electrically erasable and programmable memory cells for storing adjustment information;

memory means which is coupled for receiving the adjustment information and storing the adjustment information therein; and

peripheral circuit means which is coupled to the memory array for controlling a read operation, an erase operation and a programming operation for the memory array, wherein the peripheral circuit is further coupled to the memory means,

wherein the adjustment information stored in the second electrically erasable and programmable non-volatile memory cells is read out to the memory circuit in response to an initialization operation of the semiconductor integrated circuit device, and then operation of the peripheral circuit is controlled based upon the adjustment information stored in the memory circuit.

20. A semiconductor integrated circuit device according to claim 19,

wherein the peripheral circuit means includes an internal voltage generating means for providing internal

voltages including an erase voltage and a programming voltage, and

wherein voltage levels of the internal voltage provided from the internal voltage generator are controlled by the adjustment information.

21. A semiconductor integrated circuit device according to claim 19, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit device.

22. A semiconductor integrated circuit device according to claim 19,

wherein the memory means is a register.